In claim 3, line 14, after the second occurrence of "least" insert --one--;

In claim 5, line 1, after "said" insert --at least one--;

In claim 6, line 1, after "said" insert --at least one--;

In claim 7, line 1, after "said" insert --at least one--;

In claim 8, line 1, after "said" insert --at least one--;

In claim 9, line 1, after "said" insert --at least one--; and

In claim 10, line 1, after "said" insert --at least one--.

SUB G4 11. (amended) A method of producing a bipolar transistor for the dissipation of electrostatic discharges, comprising:

providing an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said substrate active area;

depositing a first barrier layer substantially covering said at least one thick field oxide area, said at least one active area, and said at least one transistor gate member;

planarizing said first barrier layer to expose said at least one transistor gate member;

patterning a first etch mask on said first barrier layer, wherein said first [resist] barrier layer includes openings substantially over said at least one drain region and over said at least one source region;

etching said first barrier layer to expose said at least one drain region and said at least one source region in said substrate forming at least one drain via and at least one source via, respectively;

removing said first etch mask;

depositing a layer of first conductive material over said first etched barrier layer to fill said at least one drain via and said at least one source via;

planarizing said layer of first conductive material forming at least one drain contact plug and at least one source contact plug in said at least one drain via and said at least one source via, respectively;

patterning a first deposition material on said first [buffer] barrier layer and said at least one transistor gate member, wherein said first deposition material includes openings over said at least one drain contact plug and said at least one source contact plug;

depositing a layer of second conductive material over said first deposition material to fill said openings over said at least one drain contact plug and said at least one source contact plug;

planarizing said layer of second conductive material to said first deposition material to form at least one drain contact land and at least one source contact land;

removing said first deposition material;

depositing a second barrier layer over said first barrier layer and said at least one drain contact land and at least one source contact land;

patterning a second etch mask on said second barrier layer, wherein said second [resist] barrier layer includes openings substantially over said at least one drain contact land and over said at least one source contact land;

etching said second barrier layer to expose said at least one drain contact land and said at least one source contact land forming at least one drain contact via and at least one source drain via, respectively;

removing said second etch mask;

depositing a layer of third conductive material over said etched second barrier layer to fill said at least one drain contact via and said at least one source contact via; and

planarizing said layer of third conductive material forming at least one upper drain contact and at least one upper source contact in said at least one drain contact via and said at least one source contact via, respectively.

12. (amended) The method of claim 11, further comprising:

patterning a second deposition material on said second [buffer] barrier layer, said at least one upper drain contact, and said at least one upper source contact, wherein said first deposition material includes openings over said at least one upper drain contact and said at least one upper source contact;

depositing a layer of fourth conductive material over said second deposition material to fill said openings over said at least one upper drain contact and said at least one upper source contact;

planarizing said layer of fourth conductive material to said second deposition material to form a drain contact metallization and a source contact metallization; and

removing said second deposition material.

In claim 13, line 1, before "source" insert --at least one--;

In claim 14, line 1, before "drain" insert --at least one--;

In claim 15, line 1, before "source" insert --at least one--;

In claim 16, line 1, before "drain" insert --at least one--;

In claim 17, line 1, before "upper" insert --at least one--;

In claim 18, line 1, before "upper" insert --at least one--;

In claim 20, line 5, before "active" insert --at least one--;

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21. (amended) A semiconductor device including at least one bipolar transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer substantially covering said at least one thick field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through [a] said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one implanted drain region on said semiconductor substrate;

at least one source contact plug extending through [a] said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one implanted source region on said semiconductor substrate;

at least one drain contact land disposed atop said at least one drain contact plug, wherein said at least one drain contact land has a larger cross-sectional area than said at least one drain contact plug;

at least one source contact land disposed atop said at least one source contact plug, wherein said at least one source contact land has a larger cross-sectional area than said at least one source contact plug;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, wherein said at least one upper source contact is in electrical communication with said at least one source contact land; and

at least one upper drain contact extending through said second barrier layer, wherein said at least one upper drain contact is in electrical communication with said at least one drain contact land.

In claim 23, line 1, before "source" insert --at least one--;

In claim 24, line 1, before "drain" insert --at least one--;

In claim 25, line 1, before "source" insert --at least one--;